CLAIMS

What is claimed is:

1. A method comprising:

selectively enabling or disabling outputs of voltage regulator controllers in an electronic appliance based at least in part on settings stored in non-volatile memory.

2. The method of claim 1, wherein the settings stored in non-volatile memory comprise a series of delay times assigned to voltage regulator controllers.

3. The method of claim 1, wherein the outputs of the voltage regulator controllers provide operating voltages to one or more components selected from the group consisting of a microprocessor, a chipset, a memory controller, a graphics controller, a system memory, an input/output (I/O) controller and an I/O device.

4. The method of claim 1, wherein the non-volatile memory comprises at least one memory selected from the group consisting of read only memory (ROM), flash memory, battery-backed static random access memory (SRAM), and electrically erasable programmable ROM (EEPROM).

5. The method of claim 1, further comprising locking out a power supply until the voltage regulator controller outputs are stable.

6. The method of claim 1, further comprising retrieving delay times for a future power state change.

7. An electronic appliance, comprising:

a power supply;

an electronic circuit board coupled with the power supply; and

a sequencer engine coupled with the electronic circuit board, the sequencer engine to sequentially enable voltage regulator controllers on the electronic circuit board during a power up based at least in part on settings stored in non-volatile memory.

8. The electronic appliance of claim 7, further comprising:

the sequencer engine to retrieve delay times for a future power state change.

9. The electronic appliance of claim 7, further comprising:

the sequencer engine to sequentially disable voltage regulator controllers on the electronic circuit board during a power down based at least in part on settings stored in non-volatile memory.

10. The electronic appliance of claim 7, further comprising:

the sequencer engine to lock out the power supply until the voltage regulator controller outputs are stable.

11. A storage medium comprising content which, when executed by an accessing machine, causes the accessing machine to selectively enable or disable outputs of voltage regulator controllers based at least in part on settings stored in non-volatile memory.

12. The storage medium of claim 11, wherein the settings stored in non-volatile memory comprise a series of delay times assigned to the voltage regulator controllers.

13. The storage medium of claim 11, wherein the outputs of the voltage regulator controllers provide operating voltages to one or more components selected from the group consisting of a microprocessor, a chipset, a memory controller, a graphics controller, a system memory, an input/output (I/O) controller and an I/O device.

14. The storage medium of claim 11, further comprising content which, when executed by the accessing machine, causes the accessing machine to lock out a power supply until the voltage regulator controller outputs are stable.

15. The storage medium of claim 11, further comprising content which, when executed by the accessing machine, causes the accessing machine to retrieve delay times for a future power state change.

16. An apparatus, comprising:

a non-volatile memory interface;

a power supply interface;

a voltage regulator controller interface; and

control logic coupled with the non-volatile memory, power supply and voltage regulator controller interfaces, the control logic to retrieve delay times from non-volatile memory and to enable voltage regulator controller outputs at expiration of associated delay times in response to a power up request.

17. The apparatus of claim 16, further comprising control logic to disable voltage regulator controller outputs at expiration of associated delay times in response to a power down request.

18. The apparatus of claim 16, further comprising control logic to retrieve ramp rate settings from non-volatile memory and to set voltage regulator controller output ramp rates.

19. The apparatus of claim 16, further comprising control logic to retrieve delay times for a future power state change.